

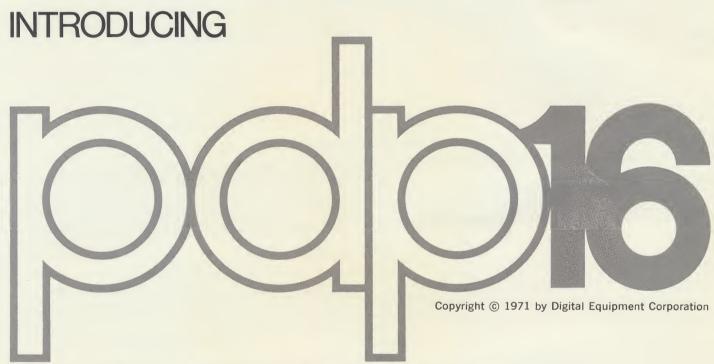
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computer designed by computer

PDP-16 is a low-cost, functional logic system defined by you and designed through "Chartware", a technique that lets our PDP-10 computer design your computer. PDP-16 will change the way you think of computers.

FEATURES

No logic design - Chartware interprets your problem and generates the right logic design, hardware requirements, and system price

Low-cost -- typical systems run from \$800-\$3,000

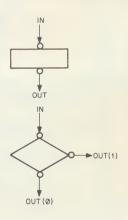




PDP-16 is Digital's design-as-you-define approach to building logic systems. Five familiar symbols are all that are needed to describe system operation. Digital takes it from there and builds the system the user has almost effortlessly designed.

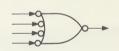
The symbols used in this shorthand approach represent actual pieces of hardware. Therefore once the user has indicated the operations which the system will perform, and the sequence of these operations, Digital can easily determine details such as module locations and pin assignments. Even if the user cannot handle the symbology, Digital can configure the system.

FLOWCHART SYMBOLS

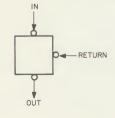


The evoke symbol represents one complete operation. For example, a single command could be coded in the following form: R1←A+B. This single command adds a 16-bit register A to a 16-bit register B and then transfers the result to register 1.

The branch symbol represents the decision to modify a control sequence depending on the logic state of the condition input.



The merge symbol represents the connection of evoke or branch outputs into a common path. This symbol is the same as the familiar OR gate of solid state logic. An OR gate arrangement is needed because outputs cannot be wired together directly.



The subroutine symbol represents a pause for the completion of a subroutine. A subroutine is a group of evoke and/or branch units used by more than one section of a program.



The terminator symbol represents the last operation of a broken control chain. No hardware is needed to carry out its function.

Once the user understands the symbology, flowcharting a PDP-16 system is quite simple. The first step, of course, is to define the problem. Then determine the necessary transfer steps and flowchart them using the symbols permitted by PDP-16 architecture.

EXAMPLE

There are two parts to Chartware - the system flowchart you provide and the system design our PDP-IO computer calculates. For example, assume you need to take input data from switches, divide it by eight and store it in one of two locations depending on whether the original data was positive or negative.

This application will need three storage locations:

- TR used to hold the number. Also performs the shift operation upon output.
- LI Destination of positive numbers.
- L2 Destination of negative numbers.
 The application will also need the switches which are inputing data.

Following are the procedures represented by the flow chart:

STEPS

- (I) Transfer data from the switches into the TR storage location.
- (2) Is the number positive?
 YES: Go to step 3
 NO: Go to step 5
- (3) Transfer a O to location L2
- (4) Transfer the contents of location TR to location LI. A divide-by-8 operation takes place during this transfer. Then return to step I.
- (5) Is the number negative?
 YES: Go to step 6
 NO: Go to step 1
- (6) Transfer a O to location LI
- (7) Transfer the contents of location RT to location L2. A divide-by-8 operation takes place during this transfer. Then return to step I.

After we receive your Chartware flowchart information, the PDP-IO:

- I) Determines the number of socket locations required for this system THERE ARE 16 SOCKETS IN THE SYSTEM WITH 12 AVAILABLE FOR USE. THEY ARE:A3-8,B3-8
- 2) Creates the bussing instructions that are unique for this configuration
 BUS THE FOLLOWING FINS:

Albert Cleur Fight, all kill minniples is share to the Föllovine sockets. A 3 10 $^\circ$ A 7

A1,B1,C1,D1, AND E1 ON SOCKE1S; B 3 TO B 7

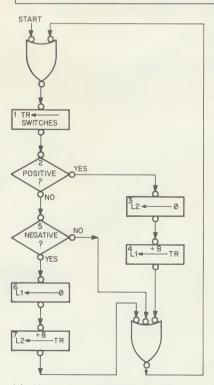
Calculates the system power requirements

TOTAL TYPICAL SYSTEM CURRENT IS 8-14 AMPS A +5 VOLT 2-782 AMP POWER SUPPLY IS RECOMMENDED.

4) Generates pin assignments for all elements needed in the system and then produces a complete wiring list (not shown)

SYMBOLIC NAME	CIRCUIT AND LOCATION	PIN ASSIGNMENTS
1	EV IN A 8	IN: U2 OUT: V2
2	B2 IN B 8	IN: H1 COND: F1 EV1: D2 EV0: E2
3	52 IN B 8	IN: K1 COND: J1 EV1: F2 EV0: H2
Z <u>i</u>	EV IN A 8	IN: E2 OUT: F2
5	EV IN A 8	IN: K2 OUT: L2
6	EV IN A 8	IN: S2 OUT: T2
7	EV IN A 8	IN: H2 OUT: J2
8	0114 IV A 8	IN: V1 U1 P1 m1 OUT: 51
9	0h4 IV A 8	IN: J1 K1 L1 M1 OUT: N1

5) Finally, calculates a system quotation SYSTEM PRICE- \$800.00



If the input data is zero, registers LI and L2 are unchanged.

The following basic arithmetic and logic functions are available in the PDP-16. Other functions can be implemented by combining two or more of these operations with the proper control logic:

Abbreviation	Definition	Description
A + B	Addition	Registers A and B are added in two's complement binary.
A - I	Decrement A	Binary I is subtracted from register A.
B	Complement B	One's complement of B is formed. (I's become O's, O's become I's.)
Ā	Complement A	One's complement of A is formed.
A + I	Increment A	Binary I is added to register A.
A × 2	A left shift	Register A is shifted left one position (in effect, multiplied by 2).
A ¥ B	Exclusive OR	Exclusive OR of A and B is formed.
AVB	Logical OR	Inclusive logical OR of A and B is formed.
АВ	Logical AND	Logical AND of A and B is formed.
A - B	Subtraction	Register B is subtracted from Register A in binary (two's complement form).
S/2	Right shift sum	One of the above functions is necessary with this command. The result is shifted one place to the right (in effect, divided by 2).

As an example of forming other functions, the two's complement of a number is generated in two steps:

A+I

First, form one's complement of A

Then, add a binary I to the result

OTHER AVAILABLE OPERATIONS

- · More complicated tasks such as bit masking or bit mapping
- · Detection of positive, zero, or negative two's complement binary numbers
- · Hardwired data constants for arithmetic or logical operations
- . Input and output buffers and control flip-flops for I/O operations

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